SİVAS UNIVERSITY OF SCIENCE AND TECHNOLOGY

FACULTY OF ENGINEERING AND

NATURAL SCIENCES

ELECTRONICS 1

Experiments Manual

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SİVAS 2026

EXPERIMENT 1: Schematic Capture and Virtual Instruments in Proteus

1. Objective of the Experiment

To establish a reproducible Proteus workflow by drawing, checking, simulating, and instrumenting a current-limited LED circuit. Delivery note: the first circuit is drawn and simulated together with the instructor; the parameter variations in Part C and the fault finding in Part D are carried out as group work; the results are evaluated jointly at the end of the session.

Learning outcomes

- Place and parameterize electronic components using meaningful reference designators.
- Connect DC sources, ground, meters, and an oscilloscope without creating floating nodes.
- Verify Kirchhoff's voltage law and compare hand calculations with simulation.
- Diagnose common schematic and simulation errors systematically.

2. Theoretical Background

A circuit simulator solves a mathematical model of the schematic. It does not infer missing ground references, correct a reversed diode, or protect an LED from excessive current. The schematic must therefore express both electrical connectivity and component parameters unambiguously.

LED current limiting

For a series LED circuit, the first estimate is I = (VS - VLED)/R. The LED voltage is not a universal 0.7 V constant; it depends on material, current, temperature, and the selected device model. KVL provides the independent check VS ≈ VR + VLED.

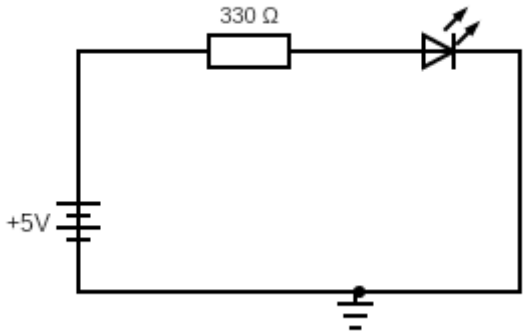


Figure 1. Series LED circuit used in the experiment.

3. Materials Used

Item	Minimum quantity / setting	Purpose
Computer with Proteus 8 or equivalent	1 per group	Schematic capture and simulation
Virtual DC source and ground	5.00 V	Excitation and reference
Red LED model	1	Nonlinear load
Resistors	330 Ω, 680 Ω, 1 kΩ	Current sweep
Virtual voltmeter, ammeter, oscilloscope	As required	Measurements

4. Procedure

Part A - Interface and file discipline

1. Create a new project folder named E1_GroupXX. Save the schematic before placing components.
2. Locate Component Mode, Terminals Mode, Instruments Mode, the wiring tool, and the simulation controls. Record the Proteus version.
3. Place a DC source, ground, one red LED, one 330 Ω resistor, a DC ammeter, and two voltmeters. Assign reference designators and values.

Part B - Calculation and first simulation

4. Assume VLED = 1.8 V and calculate the expected current for R = 330 Ω. Do not run the simulation yet.
5. Wire the series circuit in Figure 1. Put the ammeter in series. Put the voltmeters across the resistor and LED.
6. Run the simulation. If it fails, stop and use the diagnostic checklist below. Record VS, VR, VLED, and I.
7. Calculate the KVL residual |VS − VR − VLED| and the percentage difference: |Isim − Icalc| / Icalc × 100%.

R (Ω)	Icalc (mA)	Isim (mA)	VR (V)	VLED (V)	KVL residual (V)	Difference (%)
330						
680						
1000						
Student choice (220 Ω–2.2 kΩ): ____						

Part C - Parameter sweep and oscilloscope use

8. Repeat the measurement for 680 Ω and 1 kΩ without redrawing the project. Save a screenshot for each state.
9. Replace the DC source with a pulse source: low = 0 V, high = 5 V, period = 10 ms, pulse width = 5 ms (100 Hz, 50% duty cycle). Connect oscilloscope CH-A to the source and CH-B across the LED.
10. Set time base and vertical scales so that at least three full periods are visible. Measure frequency, high level, and duty cycle with cursors.
11. Explain why the LED waveform is not a scaled copy of the source waveform.

Part D - Controlled fault finding

12. Save a working copy. Introduce one fault at a time: remove ground; reverse the LED; leave a wire visibly close but electrically unconnected; and replace 330 Ω with 33 Ω.
13. For each fault, record the symptom, the most useful diagnostic observation, and the correction. Restore the verified circuit after every case.

Fault	Observed symptom	Diagnostic evidence	Correction
Missing ground			
LED reversed			
Open wire / unjoined node			
Resistance entered incorrectly			

5. Evaluation of Results

Required submission

- One annotated schematic screenshot.

- Completed current-sweep and fault-diagnosis tables.
- One oscilloscope screenshot with scales and measurement cursors visible.

Discussion questions

1. Does the simulated LED forward voltage remain constant as the current changes? Support the answer with your data.

   Response:

   _____

   _____

2. Which result gives the strongest independent evidence that the circuit is wired correctly: LED illumination, current, or the KVL residual? Explain.

   Response:

   _____

   _____

3. Why is a ground terminal necessary even when the drawn loop appears closed?

   Response:

   _____

   _____

4. What current would flow if the 330 Ω resistor were accidentally entered as 33 Ω, using VLED = 1.8 V? Is the condition acceptable?

   Response:

   _____

   _____

6. Safety Precautions

- This experiment is simulated, but use component ratings and current limiting as if the circuit were physical.
- Never transfer an unverified simulated design directly to hardware.
- Do not use unlicensed software or unknown component libraries in assessed work.

7. References

1. Labcenter Electronics, Proteus Tutorials and Learning Resources.
2. University of Minnesota, Lab 3: Analog Electronics, 2023.
3. R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed., 2012.
4. T.C. Ministry of National Education, Elektronik Elemanlar ve Devre Teorisi, course textbook

EXPERIMENT 2: Proteus Analysis, Parameter Sweeps, and Troubleshooting

1. Objective of the Experiment

To use graph-based analysis and controlled fault insertion to evaluate a loaded voltage divider and document simulation evidence.

Learning outcomes

- Configure a DC sweep and label axes with correct quantities and units.
- Quantify loading error and resistor tolerance effects.
- Distinguish loading, tolerance, and schematic faults using calculated and simulated evidence.
- Prepare a compact technical result containing a circuit, graph, table, and conclusion.

2. Theoretical Background

For an unloaded divider, Vout = Vin R2/(R1+R2). A measurement instrument or load RL changes the lower branch to R2 || RL. The loaded output is therefore smaller unless RL is much greater than R2. A sweep reveals behavior over a range and is more informative than a single operating point.

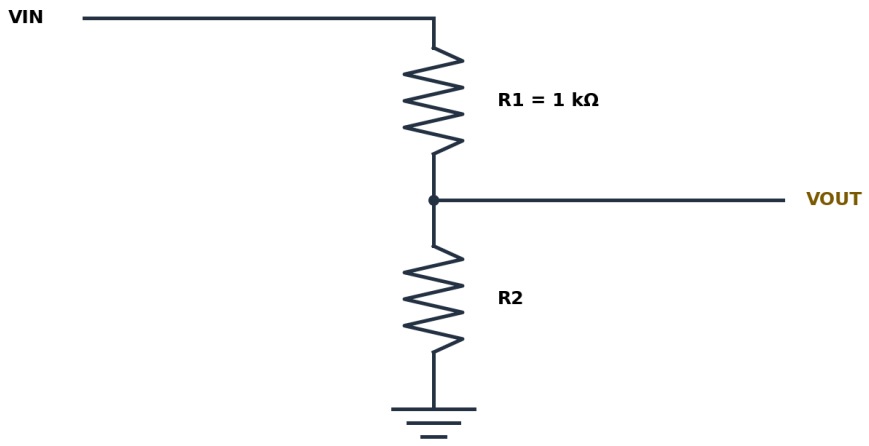


Figure 1. Divider used for DC sweep and loading analysis.

3. Materials Used

Item	Minimum quantity / setting	Purpose
Proteus or similar SPICE-capable software	1 computer	DC sweep and graphing
DC source	0-10 V sweep	Independent variable
R1	1 kΩ	Upper divider resistor
R2 values	1 kΩ, 2.2 kΩ, 4.7 kΩ, 10 kΩ	Parameter sweep
Load resistor RL	10 kΩ	Loading experiment
Voltage probes / graph	2	Vin and Vout traces

4. Procedure

Part A - Baseline divider

1. Draw Figure 1 with R1 = 1 kΩ and R2 = 2.2 kΩ. Name the source node VIN and output node VOUT.
2. Calculate Vout for Vin = 5 V and 10 V. Run two operating-point simulations and compare.
3. Confirm that current calculated from R1 agrees with current calculated from R2 within rounding error.

Part B - DC sweep

1. Place voltage probes on the VIN and VOUT nodes.
2. Select Graph Mode and place a DC Sweep graph on the schematic.
3. Open the graph properties and select the VIN source as the swept variable.
4. Set the sweep from 0 V to 10 V with a 0.1 V increment, or use at least 101 points.
5. Add V(VIN) and V(VOUT) as graph traces.
6. Run or refresh the graph and verify the axis quantities and units. Keeping R1 = 1 kΩ fixed, repeat the DC sweep for R2 = 1 kΩ, 2.2 kΩ, 4.7 kΩ, and 10 kΩ. Obtain the simulated slope from ΔVout/ΔVin and calculate the percentage difference as |msim − mtheory| / |mtheory| × 100%.

R2 (kΩ)	Theoretical slope	Simulated slope	Vout at 10 V	Difference (%)
1.0				
2.2				
4.7				
10				

Part C - Loading and tolerance

1. Return to R2 = 2.2 kΩ and connect RL = 10 kΩ from VOUT to ground. Calculate the parallel equivalent before simulation.
2. Repeat the sweep and quantify the loading error at Vin = 10 V.
3. Remove RL and set Vin to 10 V before the tolerance study. Then change R1 and R2 by +5% and −5% in the combinations that maximize and minimize Vout. Record the output range.

Case	R1 (Ω)	R2 (Ω)	RL (Ω)	Calculated Vout (V)	Simulated Vout (V)
Nominal unloaded	1000	2200	Open		
Nominal loaded	1000	2200	10000		
Worst-case high			Open		
Worst-case low			Open		

Part D - Debugging and result sheet

1. Create four faulty copies: missing ground, floating load, source polarity reversed, and a resistor entered with the wrong multiplier (for example 2.2 Ω instead of 2.2 kΩ).
2. Predict the symptom before running each faulty circuit, then compare prediction with the actual message or waveform.
3. Export one correctly labeled graph. Write a 100-150 word conclusion that states the measured slope, loading error, and dominant fault-detection lesson.

Fault	Prediction before run	Actual evidence	Root cause and fix
Missing ground			
Floating load			
Reversed source			
Wrong multiplier			

5. Evaluation of Results

Discussion questions

1. Derive the loaded-divider expression using R2 || RL.

   Response:

   _____

   _____

2. At what minimum RL/R2 ratio is the loading error below approximately 1%? Show the calculation.

   Response:

   _____

   _____

3. Why can a simulation produce a plausible graph even when the chosen component value is physically unreasonable?

   Response:

   _____

   _____

4. Which information must accompany a graph so another student can reproduce it?

   Response:

   _____

   _____

6. Safety Precautions

- Treat high simulated currents as design failures, not harmless software output.
- Save a verified baseline before fault insertion to avoid submitting a corrupted design.
- Use explicit SI prefixes; confusing m, k, M, and meg can change a result by orders of magnitude.

7. References

1. Labcenter Electronics, Graph Based Simulation and Tutorials.
2. MIT OpenCourseWare 6.002, Circuits and Electronics course materials.
3. R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed., 2012.

4. T.C. Ministry of National Education, Elektronik Elemanlar ve Devre Teorisi, course textbook.

EXPERIMENT 3: Breadboard Prototyping, Measurement, and Fault Diagnosis

1. Objective of the Experiment

To translate a verified schematic into a physical breadboard circuit and measure voltage, current, continuity, and resistance safely.

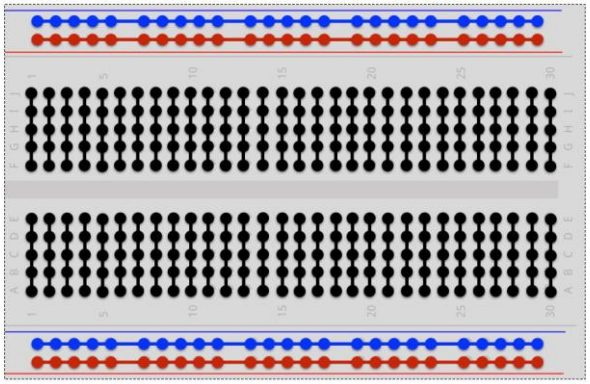
Learning outcomes

- Identify internally connected breadboard groups and split power rails.
- Build a compact LED circuit using color-coded wiring.
- Connect a DMM correctly for voltage and current measurements.
- Locate open-circuit, wrong-row, polarity, and rail-discontinuity faults.

2. Theoretical Background

A breadboard is a connection system, not a schematic. Electrically common holes are hidden under the plastic, so a visually neat circuit can still be wrong. Voltage is measured in parallel; current is measured by opening the circuit and inserting the meter in series. Resistance and continuity are measured only with power removed.

Figure 1. Simplified breadboard connectivity. Verify the actual board because some power rails are split.



3. Materials Used

Item	Minimum quantity / setting	Purpose
Solderless breadboard	1	Physical prototyping
Jumper-wire set	1	Node connections
Current-limited DC supply	5.00 V, limit 20 mA initially	Safe power
Digital multimeter	1-2	V, I, R, continuity
Red LED	1	Load
Resistors	330 Ω, 680 Ω, 1 kΩ	Current comparison

4. Procedure

Part A - Map the breadboard

1. Disconnect all power. Use continuity mode to identify one five-hole terminal group and both power rails.
2. Test whether each long power rail is continuous from end to end. Mark any rail break on the sketch below.
3. Choose red jumpers for +5 V, black for ground, and another color for signal nodes.

Breadboard region	Expected connectivity	Measured result	Continuous?
Upper positive rail	Horizontal		
Upper negative rail	Horizontal		
Lower positive rail	Test each segment separately		
Lower negative rail	Test each segment separately		
Terminal group A	Five holes		
Across center gap	Isolated		
Rail end-to-end	Board dependent		

Part B - Build and inspect before power

1. Measure and record the actual resistor value before inserting it into the breadboard. Build the 5 V - 330 Ω - LED - ground circuit from Experiment 1. Place the LED so its leads are not in the same connected group.
2. With power removed, verify the resistor and each wire connection separately using resistance or continuity mode. Test the LED separately in diode-test mode in both directions. Do not use a continuity beep through the complete resistor–LED path as the acceptance criterion, because DMM continuity thresholds vary.
3. Ask the instructor to approve the unpowered circuit. Set the supply to 5.00 V with a 20 mA current limit before connecting it.

Part C - Voltage and current measurements

1. Power the circuit. Measure supply voltage, resistor voltage, and LED voltage without moving the circuit wires.
2. Power off. Open the circuit between the resistor and LED, configure the DMM for current, insert it in series, then power on and measure current.
3. Power off and return the DMM lead to the voltage jack. Repeat all measurements for 680 Ω and 1 kΩ.
4. For each resistor, calculate I from VR/R and compare it with the direct current measurement.

R measured (Ω)	VS (V)	VR (V)	VLED (V)	I = VR/R (mA)	DMM current (mA)	Difference (%)
330 nominal						
680 nominal						
1 k nominal						

Part D - Fault diagnosis

1. With power off, allow another group member to insert one instructor-approved fault: LED reversed, resistor lead moved one row, split rail not bridged, or supply ground omitted.
2. Diagnose the circuit using a measured sequence: supply first, then node voltages, then continuity with power off. Do not randomly move wires.
3. Record the fault and the measurement that isolated it. Restore and retest the circuit.

Injected fault	First symptom	Measurement sequence	Decisive measurement	Correction

5. Evaluation of Results

Discussion questions

1. Why can the LED remain off even when 5 V is present somewhere on the breadboard?

   Response:

   _____

   _____

2. Compare direct and indirect current measurements. Which method disturbed the circuit more?

   Response:

   _____

   _____

3. What does a near-zero voltage across the resistor imply when the LED is off? Give at least two possible causes.

   Response:

   _____

   _____

4. Explain why resistance mode must not be used on an energized circuit.

   Response:

   _____

   _____

6. Safety Precautions

- Switch off the supply before changing wiring or meter function.
- Never place a DMM in current mode directly across a power supply.
- Start with a 20 mA current limit and increase only if the circuit design requires it.
- Keep clipped component leads and loose wires away from energized rails.

7. References

1. University of North Carolina, Physics 351 Electronics Laboratory Syllabus.
2. SparkFun Education, How to Use a Breadboard.
3. R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed., 2012.
4. T.C. Ministry of National Education, Elektronik Elemanlar ve Devre Teorisi, course textbook.

EXPERIMENT 4: Through-Hole Soldering, Rework, and Joint Inspection

1. Objective of the Experiment

To form, inspect, electrically verify, and rework through-hole solder joints on perfboard before assembling a functional LED circuit.

Learning outcomes

- Prepare and tin an iron safely.
- Produce repeatable joints that wet both pad and lead.
- Recognize insufficient solder, cold joints, excess solder, bridges, and lifted pads.
- Use a pump and wick for controlled desoldering.

2. Theoretical Background

A reliable joint requires clean surfaces, sufficient heat at both the pad and component lead, suitable flux, and only enough solder to form a smooth fillet. Solder is not structural glue. A visually acceptable joint must also pass electrical continuity and short-circuit checks.

Figure 1. Inspect the shape and wetting of each solder joint. Do not judge joint quality only by surface brightness, because lead-free solder may appear dull even when properly soldered.

3. Materials Used

Item	Minimum quantity / setting	Purpose
Temperature-controlled soldering station	1	Heating and soldering
Stand and brass wool / damp sponge	1	Tip control and cleaning
Perfboard	1	Practice and final circuit
Resistors / spare leads	At least 8 joints	Practice
LED and 330 Ω resistor	1 each	Functional test circuit
Electronics solder and flux	Small amount	Joint formation
Desoldering pump and wick	1 each	Rework
Safety glasses and fume extraction	1 per user / station	Protection
Digital multimeter	1	Continuity and voltage/current checks
Current-limited DC supply	5 V; 20 mA initial limit	Safe functional test

4. Procedure

Part A - Setup and dry practice

1. Put on eye protection, start local fume extraction, place the iron in its stand, and clear flammable items.
2. Identify the component side and copper-pad side of the perfboard. Plan the LED circuit before inserting parts.

3. With the station at the approved temperature, clean and lightly tin the tip. The tip should carry a thin solder film, not a large bead.

Part B - Eight-joint practice set

1. Insert four resistors, providing eight lead-to-pad joints, or use eight separate spare-wire ends. Slightly bend the leads to hold them; do not flatten them against the board.
2. Touch the tip so it contacts pad and lead simultaneously for about 1-2 s; feed solder to the heated joint, not directly to the tip.
3. Remove solder, then the iron. Let the joint cool without movement. Repeat until at least eight joints are complete.
4. Inspect each joint under good lighting. Record wetting, fillet shape, solder amount, and any defect.

Joint	Wets pad?	Wets lead?	Fillet / amount	Continuity	Bridge to neighbor?	Accept / rework
1						
2						
3						
4						
5						
6						
7						
8						

Part C - Deliberate rework

1. Select two noncritical practice joints. Remove the first using a pump and the second using solder wick.
2. Inspect the pad after each method. If the pad begins lifting, stop; do not continue heating.
3. Reinsert or reposition the lead and create a new acceptable joint. Record which method gave better control.

Part D - Functional LED board

1. Assemble a 5 V input, 330 Ω resistor, and red LED on perfboard. Use short insulated wire links where needed.
2. Trim leads only after verifying component position. Wear eye protection and hold the waste end with needle-nose pliers so it cannot fly.
3. Before power, inspect polarity, measure resistance between supply rails, and test for unwanted continuity between adjacent pads.
4. Connect a current-limited 5 V supply. Measure LED voltage and current. Use a nonconductive probe to check for intermittent joints; switch off before touching or reworking the board.

Check	Acceptance criterion	Measured / observed	Pass?
Rail-to-rail resistance	No short circuit		
Adjacent pad isolation	No unintended continuity		
LED polarity	Matches schematic		
LED voltage	Plausible for device and current		
Circuit current	Below LED rating		

5. Evaluation of Results

Discussion questions

1. Why must the pad and lead be heated together?

   Response:

   _____

   _____

2. Which inspection sign best distinguishes a wet joint from a solder blob sitting on a pad?

   Response:

   _____

   _____

3. Compare pump and wick rework. Which creates the greater risk of prolonged heating in your hands?

   Response:

   _____

   _____

4. A joint has continuity at rest but the LED flickers when the board moves. What failure mechanism is most likely?

   Response:

   _____

   _____

6. Safety Precautions

- Always return the iron to its stand; never place it on the bench or pass it hand-to-hand.
- Use local fume extraction and avoid placing your face above the joint.
- Wear eye protection during soldering and lead trimming.
- Wash hands after handling solder and flux residues; no food or drink at the station.
- Use isopropyl alcohol only after the board and iron area are safe and free from ignition sources.

7. References

1. University of California, Berkeley, Lab 1: Soldering Practice.
5. Colorado State University, ECE 202 Soldering Lab.
6. SparkFun Education, Through-Hole Soldering.
7. R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed., 2012.
8. T.C. Ministry of National Education, Elektronik Elemanlar ve Devre Teorisi, course textbook.

EXPERIMENT 5: Perfboard Layout, Assembly, Continuity Check, and Test

1. Objective of the Experiment

To translate a simple schematic into a compact, serviceable isolated-pad perfboard layout and verify the assembled circuit safely.

Learning outcomes

- Convert a schematic into a node list before placing components.
- Plan a readable component-side layout with short links and no unintended pad connections.
- Assemble the circuit using through-hole soldering and insulated wire bridges.
- Verify continuity, isolation, polarity, and operating current before final acceptance.

2. Theoretical Background

A schematic shows electrical nodes but does not specify where parts must sit on a board. On isolated-pad perfboard, each pad is normally separate. Component leads, short bare-lead links, and insulated wire bridges create the required nodes. A correct layout must preserve the schematic connections while keeping polarity visible, conductors short, and test points accessible.

The node-list method reduces wiring mistakes. For the LED circuit, the required nodes are: N1 = +5 V and R1 input; N2 = R1 output and LED anode; N3 = LED cathode and 0 V. Every intended connection must belong to one of these nodes, and different nodes must not be directly shorted.

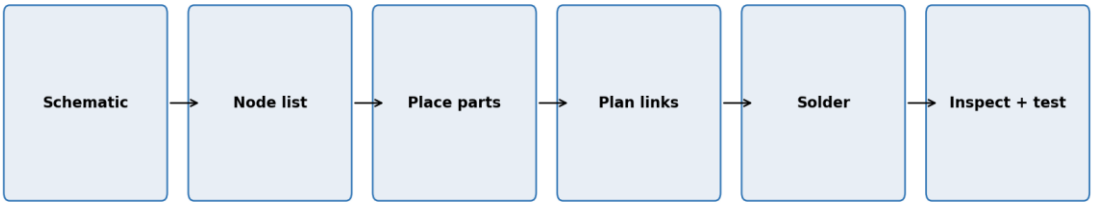


Figure 1. Schematic-to-perfboard assembly workflow.

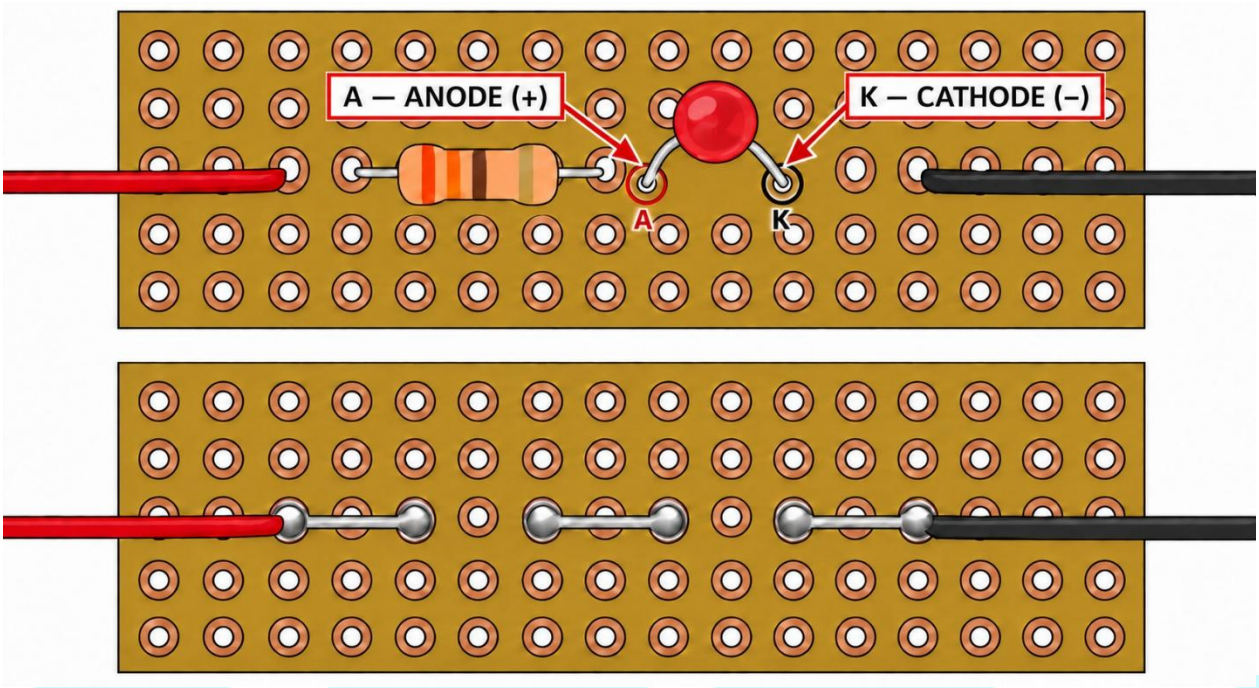


Figure 2. Component-side placement and corresponding solder-side connections, shown from the component-side viewing direction, for the series LED circuit. Students may use a different compact layout if the same nodes are preserved.

3. Materials Used

Item	Minimum quantity / setting	Purpose
Isolated-pad perfboard	Approximately 5 cm x 7 cm; 1 per group	Permanent assembly
Red LED and 330 Ω, 1/4 W resistor	1 each	Series LED circuit
Red and black insulated hookup wires	Approximately 15 cm each	+5 V and 0 V supply leads
Single-core insulated hookup wire	Approximately 30 cm	Connections and bridges
Soldering iron, stand, solder, and flux	1 station	Assembly
Side cutter, needle-nose pliers, tweezers	1 set	Lead preparation
Desoldering pump or wick	1	Correction
DMM and current-limited DC supply	5 V; 20 mA initial limit	Inspection and test

4. Procedure

Part A - Schematic, node list, and layout plan

1. Redraw the 5 V series LED circuit and label the red +5 V and black 0 V supply wires, resistor R1, and LED1. Mark the LED anode and cathode.
2. Write the three-node list N1, N2, and N3 described in the theory section. Check that each component terminal appears exactly once.
3. Place the unsoldered parts on the perfboard. Keep the supply wires at an edge, the LED visible, and at least one unused hole between unrelated conductors where practical.

4. Sketch the component-side layout in the grid below. Use solid lines for component leads and dashed lines for insulated wire links. Ask for instructor approval before soldering.

Node	Must connect	Chosen holes / route	Approved?
N1	+5 V red wire, R1 input		
N2	R1 output, LED anode		
N3	LED cathode, 0 V black wire		

Part B - Dry fit and assembly

1. Measure R1 and record its actual value. Verify LED polarity with package marking and DMM diode-test mode.
2. Insert and secure the red/black supply wires, R1, and LED1 without solder. Recheck the layout from both sides; remember that the solder-side view is mirrored.
3. Solder one terminal at a time. Form only the planned connections with short leads or insulated wire. Do not create long solder blobs between distant pads.
4. Trim leads after confirming the connections. Inspect every joint and rework bridges, insufficient wetting, or loose parts.

Part C - Unpowered tests

1. Check continuity along every intended node. Probe from the component terminal, not only from nearby solder.
2. Check for unintended shorts between adjacent pads that are not assigned to the same node. Do not use continuity between N1–N2 or N2–N3 as an isolation test, because R1 and LED1 intentionally connect those node pairs. Compare resistance and diode-test readings with the expected circuit behavior.
3. Measure resistance between the red +5 V wire and the black 0 V wire in both probe orientations. Investigate any near-zero reading before applying power.
4. Use diode-test mode to confirm LED orientation and record the indicated forward voltage if the DMM can illuminate it.

Test points	Expected	Measured	Pass?
red +5 V wire to R1 input	Continuity		
R1 output to LED anode	Continuity		
LED cathode to black 0 V wire	Continuity		
Adjacent unrelated pads	Open / no continuity		
red +5 V wire to black 0 V wire	No short circuit		
LED diode test	Forward in one direction		

Part D - Current-limited power-up and diagnosis

1. Set 5.00 V and a 20 mA current limit before connecting the board. Ask for instructor approval.
2. Power the board. Record supply current, resistor voltage, LED voltage, and brightness observation.

3. Calculate current from IR = VR/Rmeasured and compare it with the supply reading. If the supply enters current limit or the LED remains off, disconnect power and repeat the unpowered tests.
4. Gently move each insulated link with a nonconductive tool while powered. Any flicker indicates a weak joint; switch off before reworking.
5. Photograph both sides of the finished board and annotate supply-wire polarity, R1, LED1, and the three nodes.

Quantity	Calculated	Measured	Difference / comment
Supply voltage (V)	5.00		
LED current (mA)			
Resistor voltage (V)			
LED voltage (V)			

5. Evaluation of Results

Discussion questions

1. Why should the node list be completed before choosing hole positions?

   Response:

   _____

   _____

2. Why is a long solder bridge less reliable than a short insulated wire link?

   Response:

   _____

   _____

3. A circuit has correct node continuity but the LED does not light. List the next three checks in order.

   Response:

   _____

   _____

4. How does viewing the solder side as a mirror image create wiring mistakes, and how did you prevent them?

   Response:

   _____

   _____

6. Safety Precautions

- Do not apply power until visual inspection, continuity, and short-circuit checks pass.
- Use a current-limited supply for first power-up.
- Observe all soldering and lead-trimming precautions from Experiment 4.
- Do not hold the board in your hand while soldering or energizing it.
- This exercise uses low-voltage DC only; do not connect the board to mains voltage.

7. References

1. University of California, Berkeley, Lab 1: Soldering Practice.
2. Colorado State University, ECE 202 Soldering Lab.
3. SparkFun Education, Through-Hole Soldering.
4. R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed., 2012.
5. T.C. Ministry of National Education, Elektronik Elemanlar ve Devre Teorisi, course textbook.

EXPERIMENT 6: Forward and Reverse Characteristics of a Silicon Diode

1. Objective of the Experiment

To obtain the measured I-V characteristic of a 1N4148 diode, estimate its incremental resistance, and compare constant-drop, exponential, simulation, and physical results.

Learning outcomes

- Identify anode and cathode using package marking and diode-test mode.
- Measure forward current over a controlled voltage sweep without exceeding ratings.
- Plot linear and semilog I-V data and determine a local slope.
- Observe reverse blocking at a safe voltage without attempting breakdown.

2. Theoretical Background

The Shockley relation ID = IS[exp(VD/(nVT)) - 1] describes the exponential region approximately. Real devices also include series resistance, leakage, temperature dependence, and nonideal recombination. The familiar 0.7 V value is a circuit approximation, not a turn-on switch.

With a series resistor, current is obtained accurately from ID = VR/R. The local or incremental resistance around an operating point is rd ≈ ΔVD/ΔID. In reverse bias below breakdown, the current may be smaller than the resolution of an ordinary DMM.

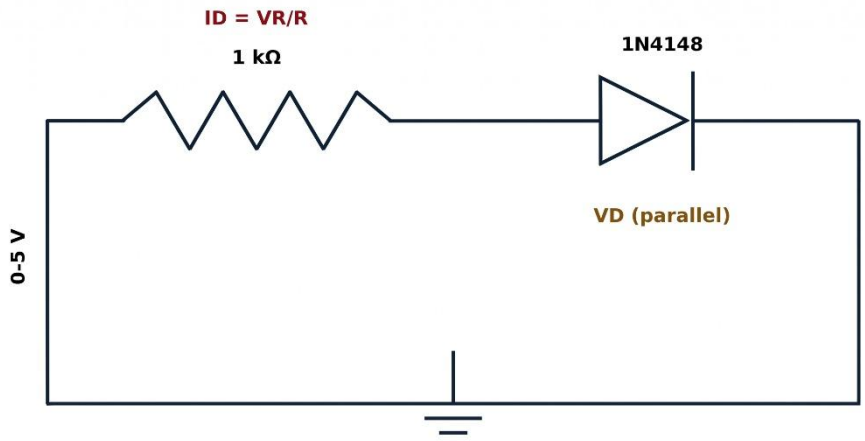


Figure 1. Forward-bias circuit. Measure current from resistor voltage to avoid moving the DMM into series for every point.

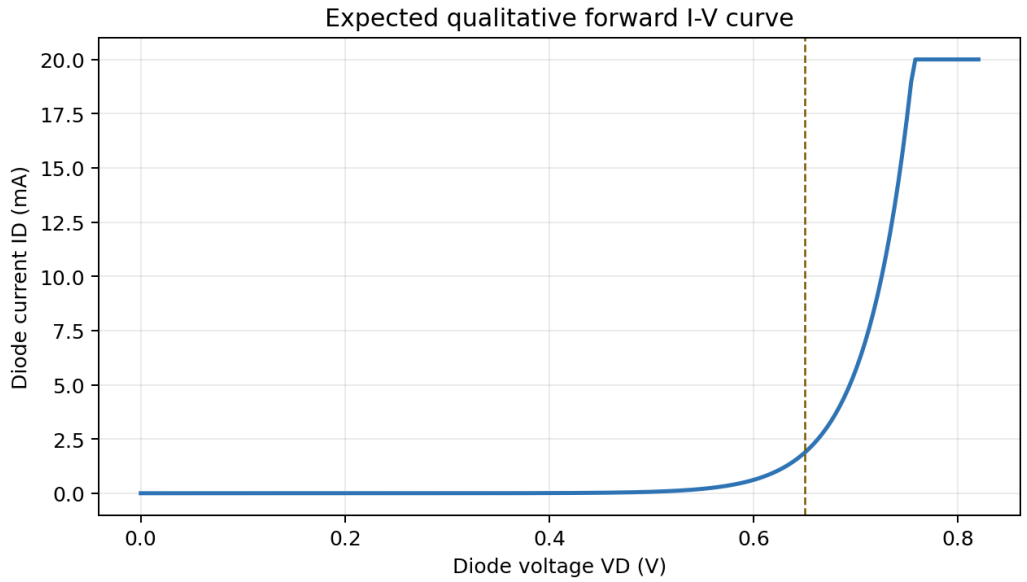


Figure 2. Qualitative forward I-V behavior; the measured curve must be plotted from student data.

3. Materials Used

Item	Minimum quantity / setting	Purpose
1N4148 diode	1	Device under test
1 kΩ resistor	1, measured value recorded	Current limiting and sensing
Adjustable current-limited DC supply	0-5 V	Sweep
DMM	2 preferred	VD and VR
Breadboard and jumpers	1 set	Construction
Proteus or similar simulator	Pre-lab / comparison	Model curve

4. Procedure

Part A - Identification and pre-check

1. Locate the cathode band. Verify polarity using DMM diode-test mode in both directions. Record the forward indication.
2. Measure the actual 1 kΩ resistor value. Calculate the maximum possible current at 5 V for a shorted diode and confirm it is safe.
3. Build Figure 1 with the supply off. Ask for a connection check.

Part B - Forward sweep

1. Set the supply to each listed value. At every point measure VS, VD, and VR after the reading stabilizes.
2. Use smaller voltage steps in the knee region. Calculate ID = VR/Rmeasured. Do not calculate current from the nominal resistor value.
3. If current exceeds 5 mA, stop the sweep unless the instructor authorizes continuation.

VS set (V)	VS measured (V)	VD (V)	VR (V)	ID = VR/R (mA)
0.00				
0.20				
0.30				

VS set (V)	VS measured (V)	VD (V)	VR (V)	ID = VR/R (mA)
0.40				
0.50				
0.55				
0.60				
0.65				
0.70				
0.75				
0.80				
0.85				
1.00				
1.50				
2.00				
3.00				
4.00				
5.00				

Part C - Curve extraction and dynamic resistance

1. Plot ID versus VD on linear axes. Create a second plot with a logarithmic current axis, excluding zero or negative current entries.
2. Select two neighboring points near ID ≈ 1 mA and calculate rd = ΔVD/ΔID.
3. Estimate the change in VD associated with a tenfold current increase where the data allow it. Compare with the ideal room-temperature trend and explain nonideality.

Point	VD (V)	ID (mA)
A		
B		

Incremental resistance rd = ΔVD/ΔID = _____ Ω

Part D - Safe reverse-bias observation and simulation comparison

1. Power off and reverse the diode. Keep the 1 kΩ series resistor.
2. Apply 1 V, 3 V, and 5 V reverse bias. Record current or the meter resolution limit. Do not attempt avalanche breakdown.
3. Return the diode to the forward-bias connection and set the simulated resistor to the measured value Rmeasured. Reuse the DC Sweep method introduced in Experiment 2. Sweep the supply from 0 to 5 V using sufficiently small increments in the knee region. Plot VD and calculate ID from the simulated resistor voltage, ID = VR/Rmeasured. Export or tabulate the simulated ID–VD data and compare it with the measured values. Then reverse the diode in the simulation and record the simulated current at 1 V, 3 V, and 5 V reverse bias so that the reverse-bias rows of the table can be completed.

Condition	VD measured (V)	ID measured / limit (µA)	ID simulated (µA)	Comment
Reverse 1 V				

Condition	VD measured (V)	ID measured / limit (µA)	ID simulated (µA)	Comment
Reverse 3 V				
Reverse 5 V				
Forward ≈0.1 mA				
Forward ≈1 mA				

5. Evaluation of Results

Discussion questions

1. Use your data to show why 0.7 V is not a fixed switching threshold.

   Response:

   _____
   _____

2. What limits the accuracy of reverse leakage measurement in this setup?

   Response:

   _____
   _____

3. Compare the diode-test indication with VD near 1 mA. Why might the values differ?

   Response:

   _____
   _____

4. How would self-heating alter the measured curve during a slow high-current sweep?

   Response:

   _____

6. Safety Precautions

- Use the series resistor at all times and set a conservative current limit.
- Switch off power before reversing the diode or changing meter connections.
- Do not attempt reverse breakdown of a 1N4148 with the available supply.
- Verify cathode marking against the actual component; do not rely on a schematic symbol alone.

7. References

1. Auburn University ELEC 2210, Diodes Laboratory.
2. University of Washington EE331, Diode Circuit Applications.
3. R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed., 2012.

EXPERIMENT 7: Half-Wave and Bridge Rectifiers with Capacitive Filtering

1. Objective of the Experiment

To compare half-wave and full-wave bridge rectification and quantify how filter capacitance and load affect DC level and ripple.

Learning outcomes

- Connect an isolated low-voltage AC source and oscilloscope with correct grounding.
- Measure peak, average, ripple, and ripple frequency.
- Compare 0, 100 µF, and 470 µF filters under two loads.
- Explain diode drop and discharge interval effects.

2. Theoretical Background

A half-wave rectifier conducts during one polarity of the input, so its ripple repetition frequency equals the source frequency. A bridge uses two conducting diodes in each half-cycle and produces a ripple repetition frequency twice the source frequency. A shunt capacitor charges near the rectified peak and discharges through the load between charging intervals.

For small ripple, Vr(pp) ≈ Iload/(fripple C). The approximation becomes inaccurate when ripple is large or conduction occupies a substantial part of the cycle. Measured waveforms should therefore be compared with both the approximation and simulation.

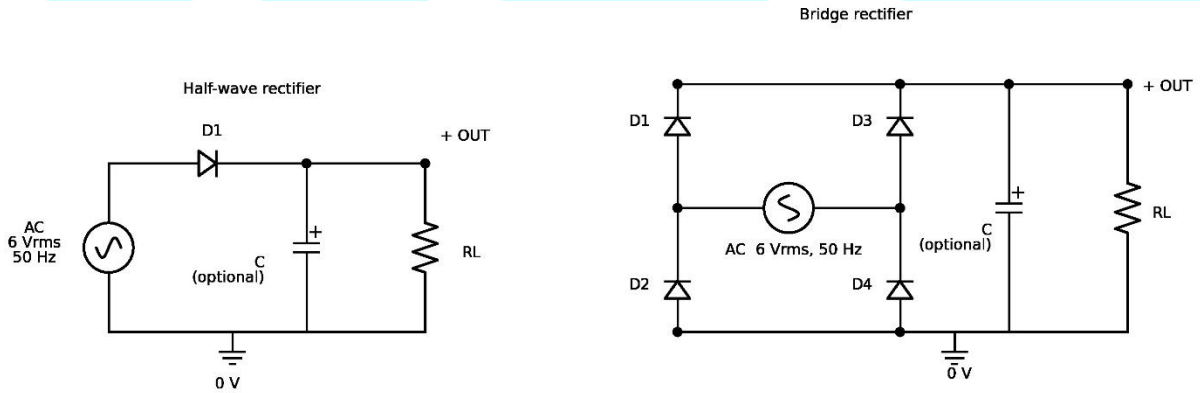


Figure 1. Half-wave and bridge rectifier topologies with the optional filter capacitor across the load. The bridge diodes are labelled D1–D4, the capacitor polarity is shown, and the positive output and 0 V nodes are marked.

3. Materials Used

Item	Minimum quantity / setting	Purpose
Isolated AC source	6 Vrms nominal, 50 Hz	Safe excitation
1N4007 diodes	4	Rectification
Load resistors	1 kΩ and 2.2 kΩ, suitable power rating	Load sweep
Electrolytic capacitors	100 µF and 470 µF, ≥25 V	Filtering
Two-channel oscilloscope	1	Waveform and ripple

Item	Minimum quantity / setting	Purpose
DMM	1	DC output
Proteus or similar simulator	Pre-lab	Comparison
Solderless breadboard and jumper wires	1 set	Safe rectifier assembly

4. Procedure

Part A - Source verification

1. Before connecting diodes, measure the isolated source with the oscilloscope and DMM. Record Vrms, Vpeak, and frequency.
2. Confirm Vpeak ≈ √2 Vrms within instrument accuracy. Set scope probes to the correct attenuation factor.

Quantity	DMM / scope result	Expected relation	Difference
Vrms		-	
Vpeak		√2 Vrms	
Frequency		Nominal 50 Hz	

Part B - Half-wave rectifier (30 min)

1. Build the half-wave circuit with RL = 1 kΩ and no capacitor. Observe input and output simultaneously.
2. Measure output peak, DC average, minimum, and ripple repetition frequency.
3. Add 100 µF with correct polarity. Measure VDC and ripple peak-to-peak using AC coupling or vertical zoom as appropriate.
4. Replace with 470 µF. Discharge the removed capacitor through a resistor before handling or measuring resistance.

Part C - Bridge rectifier

1. Power off and build the bridge. Verify all four diode polarities before connecting the source.
2. Repeat no-capacitor, 100 µF, and 470 µF measurements with RL = 1 kΩ.
3. Identify the approximate two-diode peak loss from the input peak and output peak.

Part D - Load comparison and calculations

1. Set RL = 1 kΩ, then repeat with RL = 2.2 kΩ. Use 100 µF and 470 µF for each rectifier topology.
2. For each case, measure VDC with the DMM or from the DC-coupled oscilloscope trace. Measure Vr(pp) with DC coupling and vertical zoom; AC coupling may be used only for an enlarged ripple view, and the coupling mode must be recorded.
3. Calculate the load current using Iload = VDC/RL.
4. For C > 0, calculate the expected ripple as Vr(pp) ≈ Iload/(fripple C), using fripple = 50 Hz for half-wave operation and fripple = 100 Hz for bridge operation.
5. For C = 0, record the ripple approximation and its error as N/A, because the small-ripple formula does not apply.
6. Calculate the ripple error = |Vr,measured − Vr,calculated| / Vr,calculated × 100%.
7. Save one oscilloscope screenshot for each rectifier. Each screenshot must state probe attenuation and coupling and clearly show the DC level and the peak-to-peak ripple measurement.

Topology	RL	C	Vpeak (V)	VDC (V)	Vr(pp) measured (V)	fripple (Hz)	Vr(pp) calc. (V)	Ripple error (%)
Half-wave	1 kΩ	0					N/A	N/A
Half-wave	1 kΩ	100 µF						
Half-wave	1 kΩ	470 µF						
Half-wave	2.2 kΩ	100 µF						
Half-wave	2.2 kΩ	470 µF						
Bridge	1 kΩ	0					N/A	N/A
Bridge	1 kΩ	100 µF						
Bridge	1 kΩ	470 µF						
Bridge	2.2 kΩ	100 µF						
Bridge	2.2 kΩ	470 µF						

5. Evaluation of Results

Discussion questions

1. Why is the bridge ripple frequency twice the source frequency?

   Response:

   _____

   _____

2. Why can the bridge output peak be lower than the half-wave peak even though it uses both half-cycles?

   Response:

   _____

   _____

3. For fixed load, does measured ripple vary inversely with capacitance? Quantify using your data.

   Response:

   _____

   _____

4. Why is the small-ripple approximation not applicable when C = 0, and why does its accuracy decrease under heavy loading?

   Response:

   _____

   _____

6. Safety Precautions

- Use only an instructor-provided isolated low-voltage AC source; never connect the circuit directly to mains.
- Verify electrolytic capacitor polarity and voltage rating before power.
- Power off and discharge capacitors through a resistor before rewiring.
- All channels of a standard bench oscilloscope share a common ground. When testing the bridge rectifier, never connect channel ground clips to different bridge nodes. Use one instructor-approved reference node and use a differential probe or the oscilloscope math function when a floating voltage must be measured.

7. References

1. Auburn University ELEC 2210, Diodes: Rectifier and Filter Laboratory.

2. University of Washington EE331, Diode Circuit Applications.
3. R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed., 2012.
4. T.C. Ministry of National Education, Elektronik Elemanlar ve Devre Teorisi, course textbook.

EXPERIMENT 8: Diode Clippers and Clampers

1. Objective of the Experiment

To build positive and negative diode limiters and clampers, measure their transfer behavior, and relate waveform levels to diode polarity and RC time constant.

Learning outcomes

- Predict conduction intervals before measurement.
- Measure clipping level, DC shift, and droop.
- Reverse a diode and explain the observed polarity change.
- Evaluate the condition RC >> signal period for effective clamping.

2. Theoretical Background

A clipper limits one portion of a waveform when a diode becomes forward biased. A simple silicon shunt clipper typically limits near a diode forward voltage rather than exactly 0 V. A clamper uses a diode, capacitor, and resistor to shift the waveform's DC level while approximately preserving peak-to-peak amplitude.

Clamping is effective when the capacitor charges rapidly during diode conduction and discharges slowly through the load. The ratio RC/T determines droop. Instrument input resistance becomes part of the effective load and must not be ignored.

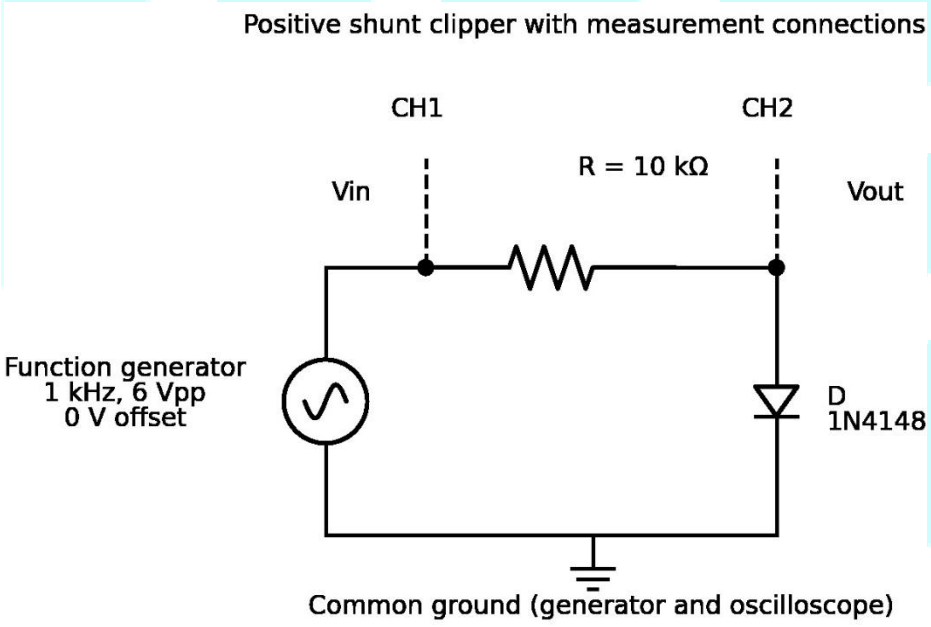


Figure 1. Representative positive shunt clipper and measurement connections.

3. Materials Used

Item	Minimum quantity / setting	Purpose
1N4148 diodes	2	Clipping and clamping
Resistors	10 kΩ and 100 kΩ	Current limit / discharge path
Capacitors	100 nF and 1 µF (non-polarized)	Time-constant comparison
Function generator	1 kHz sine and square, 6 Vpp, 0 V offset	Input
Two-channel oscilloscope	1	Waveform comparison
Adjustable DC source	1.0 V; required for Part D	Biased clipping
Breadboard and jumpers	1 set	Construction

4. Procedure

Part A - Positive and negative shunt clippers

1. Set the generator to a 1 kHz sine wave, 6 Vpp, 0 V offset. Verify the signal on the oscilloscope before connecting the circuit.
2. Build the positive shunt clipper with a 10 kΩ series resistor. Display Vin and Vout simultaneously using the same ground reference.
3. Measure positive maximum, negative minimum, Vpp, and the input voltage at which clipping begins.
4. Power down, reverse the diode, and repeat for negative clipping. Save both waveform pairs.

Circuit	Vin max	Vin min	Vout max	Vout min	Measured clip level	Predicted level
Positive clipper						
Negative clipper						

Part B - Transfer characteristic

1. Use XY mode with Vin on X and Vout on Y, or perform a slow DC sweep in simulation.
2. Identify the unity-slope region and the limited region. Record at least seven (Vin, Vout) pairs around the knee.

Point	Vin (V)	Vout (V)	Diode state
1			
2			
3			
4			
5			
6			
7			

Part C - Positive and negative clampers

1. Build a clamper using a 1 µF non-polarized capacitor, 100 kΩ, and 1N4148. If an electrolytic capacitor is authorized, power off and recheck its polarity after every diode reversal. Use a 1 kHz square wave at 6 Vpp and 0 V offset.
2. Measure Vin,max, Vin,min, Vout,max, Vout,min, Vout,pp, and mean/DC level. Determine whether the waveform is shifted up or down.
3. Reverse the diode and repeat; orientation A is the positive clamper and orientation B is the negative clamper. Then return to orientation A and replace 1 µF with 100 nF, and quantify droop over one half-cycle.
4. Calculate RC/T for both capacitors using the effective resistance Reff = RL ∥ Rscope. Express droop as % droop = |ΔVplateau| / Vout,pp × 100 and relate the ratios to the measured droop.

Diode orientation	C	RC/T	Vout max	Vout min	Vout pp	DC level	Droop (%)
Orientation A (positive clamper)	1 µF						
Orientation B (negative clamper)	1 µF						
Orientation A (positive clamper)	100 nF						

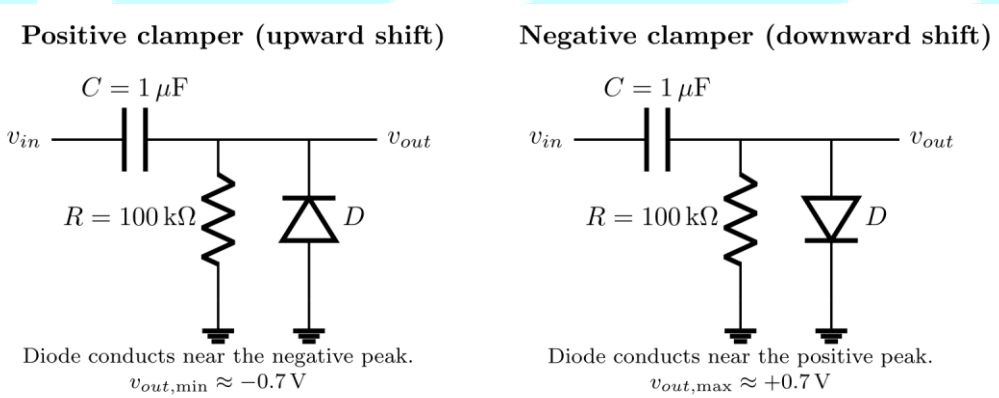


Figure 2. Positive and negative clamper connections. Reversing the diode changes the direction of the DC level shift.

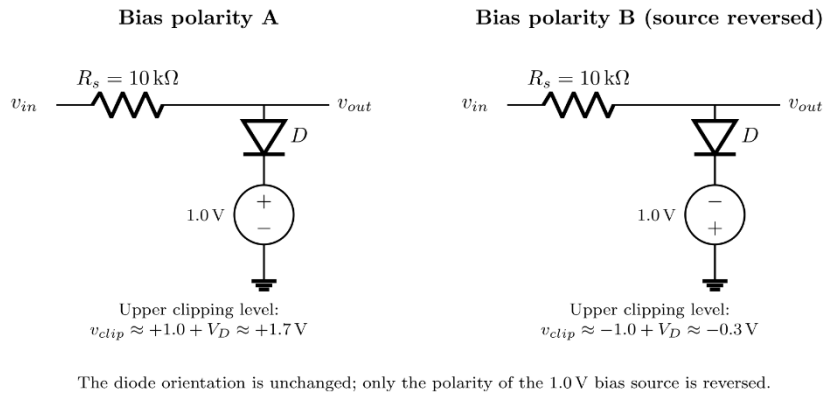


Figure 3. Biased shunt clipper with two bias-source polarities. The diode orientation remains unchanged; reversing the 1.0 V source shifts the clipping level from approximately +1.7 V to −0.3 V.

Part D - Biased clipping

1. Add the required 1.0 V DC bias source in series with the diode using the instructor-approved polarity. Keep the input at 1 kHz, 6 Vpp, and 0 V offset.
2. Predict the new clipping level including diode drop, then measure it.
3. Reverse only the bias source and explain the resulting level.

5. Evaluation of Results

Discussion questions

1. Why is the measured clipping level not exactly 0.7 V at every point?

   Response:

   _____

   _____

2. What portion of the clamper cycle produces rapid capacitor charging?

   Response:

   _____

   _____

3. Use RC/T and measured droop to justify whether each clamper meets the long-time-constant assumption.

   Response:

   _____

   _____

4. Does an ideal clamper change Vpp? Explain why the real circuit may show a small change.

   Response:

   _____

   _____

6. Safety Precautions

- Verify generator ground and oscilloscope ground share the intended circuit reference.
- Switch off the source before reversing a diode or electrolytic capacitor.
- Use the series resistor; do not connect the diode directly across a low-impedance source.
- Keep applied signals within diode and instrument ratings.

7. References

1. MIT OpenCourseWare 6.101, Diode Clippers and Clampers.
2. University of Washington EE331, Diode Circuit Applications.
3. R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed., 2012.
4. T.C. Ministry of National Education, Elektronik Elemanlar ve Devre Teorisi, course textbook.

EXPERIMENT 9: BJT Input and Output Characteristics

1. Objective of the Experiment

To measure the common-emitter input and output characteristics of a BC547 NPN transistor and identify cutoff, active, and saturation regions.

Learning outcomes

- Verify the exact BC547 pinout for the supplied package.
- Generate IC-VCE curves at several fixed base currents.
- Estimate DC current gain β in the active region.
- Recognize why β is not a device constant.

2. Theoretical Background

In forward-active operation, the base-emitter junction is forward biased and IC is approximately βIB, while VCE has a comparatively weak influence. At low VCE the transistor enters saturation and the proportional relationship degrades. At IB ≈ 0 the transistor is in cutoff except for leakage.

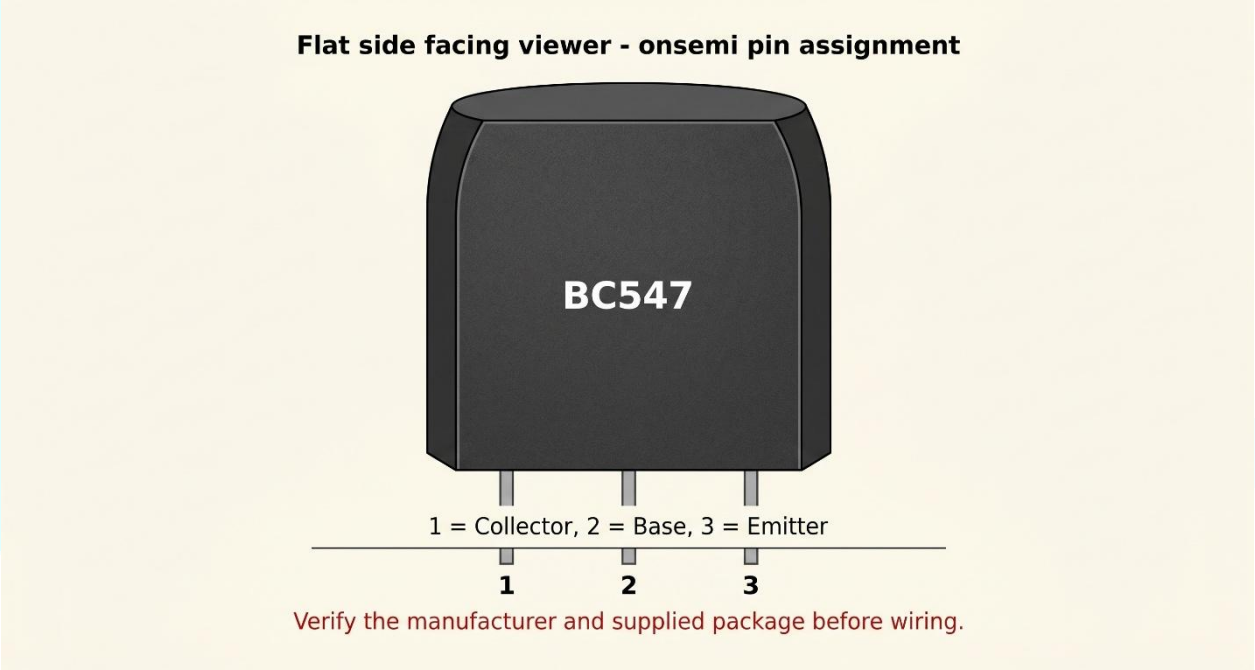


Figure 1. onsemi BC547 TO-92 pin assignment, flat side facing the viewer. Confirm the manufacturer of the supplied part.

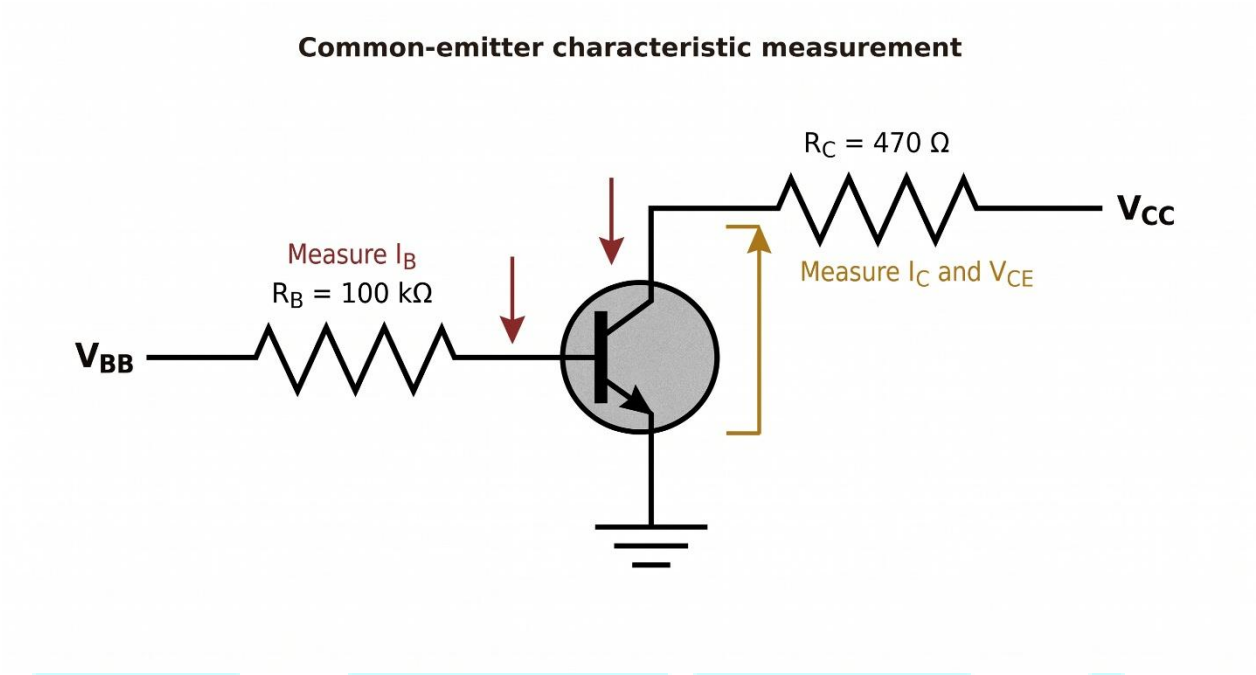


Figure 2. Two-supply common-emitter measurement concept. Use the instructor-approved source arrangement.

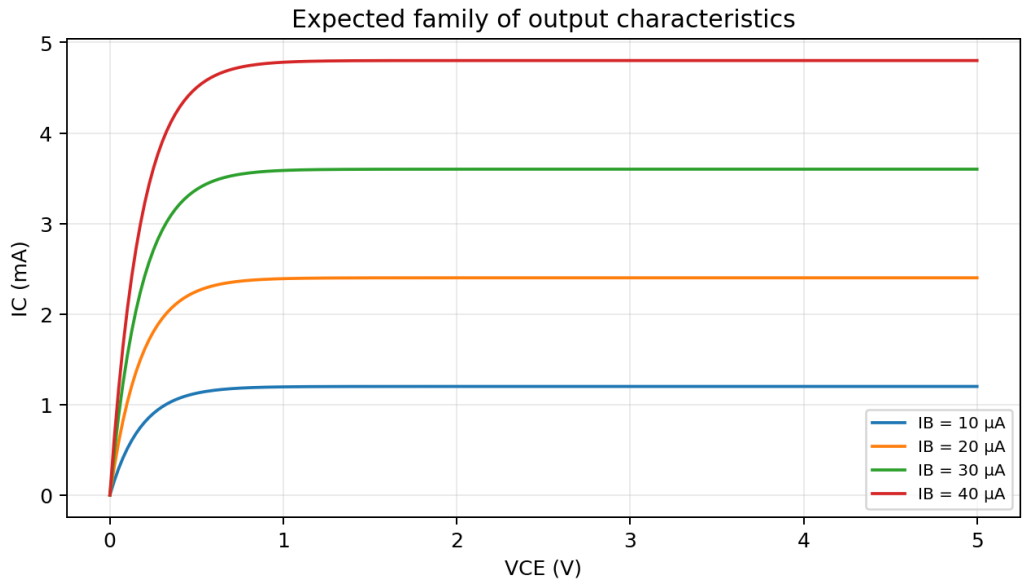


Figure 3. Qualitative output characteristic family; student curves must use measured data.

3. Materials Used

Item	Minimum quantity / setting	Purpose
BC547 NPN transistor	1-2	Device under test
Base resistor	100 kΩ	Base-current control
Collector resistor	470 Ω	Current limiting
Two adjustable DC outputs / dual supply	0–5 V; V_{CC}: 0–10 V, current-limited	Independent base-current and collector-voltage control
DMMs	2-3 preferred	IB, IC, VBE, VCE
Breadboard and jumpers	1 set	Construction
BC547 manufacturer datasheet	Exact supplied part	Pinout and ratings

4. Procedure

Part A - Pinout and junction checks

1. Record manufacturer and complete marking of the supplied BC547. Draw the package viewed from the correct side and label C, B, and E.
2. Use diode-test mode to identify base-emitter and base-collector junctions. Record forward indications and reverse open-circuit indications.
3. Measure the actual collector and base resistors.

Test	Forward indication	Reverse indication	Interpretation
Base-emitter			
Base-collector			

Part B - Input characteristic

9. Build the two-supply circuit with the VBB and VCC negative terminals connected to the emitter/ground node. Starting from zero, adjust VBB to obtain the target measured IB, then adjust VCC until the measured VCE is 2.0 V. Repeat these two adjustments iteratively because they interact.
10. At each point record IB and VBE. Do not exceed IB = 40 µA or IC = 10 mA in this experiment.
11. Plot IB versus VBE using a logarithmic vertical axis if possible.

IB target (µA)	IB measured (µA)	VBE (V)	VCE (V)
0			
5			
10			
20			
30			
40			

Part C - Output characteristic family

1. Set IB = 0 µA. Sweep VCE through 0, 0.1, 0.2, 0.5, 1, 2, 3, 4, and 5 V, recording IC.
2. Repeat the collector sweep at IB = 10, 20, 30, and 40 µA. For each point, adjust VBB and VCC alternately until the measured IB and the measured VCE are both at their target values, because changing VCE disturbs the base current. Do not exceed IC = 10 mA, VCE = 5 V, or VCC = 10 V. If a point cannot be reached within these limits, record N/A instead of forcing the setting..
3. At the highest-current point of each curve, calculate transistor power P = VCE IC. Stop if readings are unstable or any rating/limit is approached.
4. Plot all IC-VCE curves on one graph with a clear legend.

VCE (V)	IC at IB=0 µA (mA)	IC at IB=10 µA (mA)	IC at IB=20 µA (mA)	IC at IB=30 µA (mA)	IC at IB=40 µA (mA)
0					
0.1					

VCE (V)	IC at IB=0 µA (mA)	IC at IB=10 µA (mA)	IC at IB=20 µA (mA)	IC at IB=30 µA (mA)	IC at IB=40 µA (mA)
0.2					
0.5					
1					
2					
3					
4					
5					

Part D - Gain and region extraction

1. At VCE = 2 V, calculate βDC = IC/IB for each nonzero base current.
2. Estimate the knee voltage using a stated criterion, such as where IC begins to depart from the active-region curve. Do not report this graphical knee as a datasheet VCE(sat) measurement.
3. If a second BC547 is available, repeat the VCE = 2 V gain measurement at IB = 20 µA and compare device variation.

IB (µA)	IC at VCE=2 V (mA)	βDC	Region
10			
20			
30			
40			
Second device at 20			

5. Evaluation of Results

Discussion questions

1. Identify cutoff, saturation, and active regions on your measured graph.

   Response:

   _____

   _____

2. Does β remain constant with collector current? Use numerical evidence.

   Response:

   _____

   _____

3. Why must VCE be readjusted after changing VBB or IB?
   Response:
   _____
   _____

4. What physical or measurement factors can cause differences between two BC547 samples?
   Response:
   _____
   _____

6. Safety Precautions

- Confirm BC547 pinout from the actual datasheet before power.
- Use both base and collector current-limiting resistors.
- Do not exceed IB = 40 µA, IC = 10 mA, VCE = 5 V, or the instructor's lower limits.
- Power off before moving meters or transistor leads.

7. References

1. Auburn University ELEC 2210, BJT Transistors Laboratory.
2. onsemi, BC546/BC547/BC548/BC549/BC550 Datasheet.

EXPERIMENT 10: Voltage-Divider BJT Bias and Q-Point Stability

1. Objective of the Experiment

To design, measure, and perturb a voltage-divider biased BC547 stage and relate the measured Q point to Thevenin analysis and the DC load line.

Learning outcomes

- Calculate VTH, RTH, IB, IC, VE, VC, and VCE without assuming an ideal divider.
- Locate the measured Q point on a DC load line.
- Quantify sensitivity to transistor replacement and supply variation.
- Diagnose cutoff and saturation bias faults.

2. Theoretical Background

The base divider can be replaced by $VTH = VCCR2/(R1 + R2)$and RTH = R1 || R2. Including base loading, $IB \approx (VTH - VBE)/(RTH + (\beta + 1)RE)$. Then $IC \approx \beta IB$, VE ≈ IE RE, VC = VCC - IC RC, and VCE = VC - VE.

The approximate DC load-line intercepts are VCE ≈ VCC at IC = 0 and IC ≈ VCC/(RC+RE) near VCE = 0. A useful amplifier Q point lies in the active region with headroom in both directions.

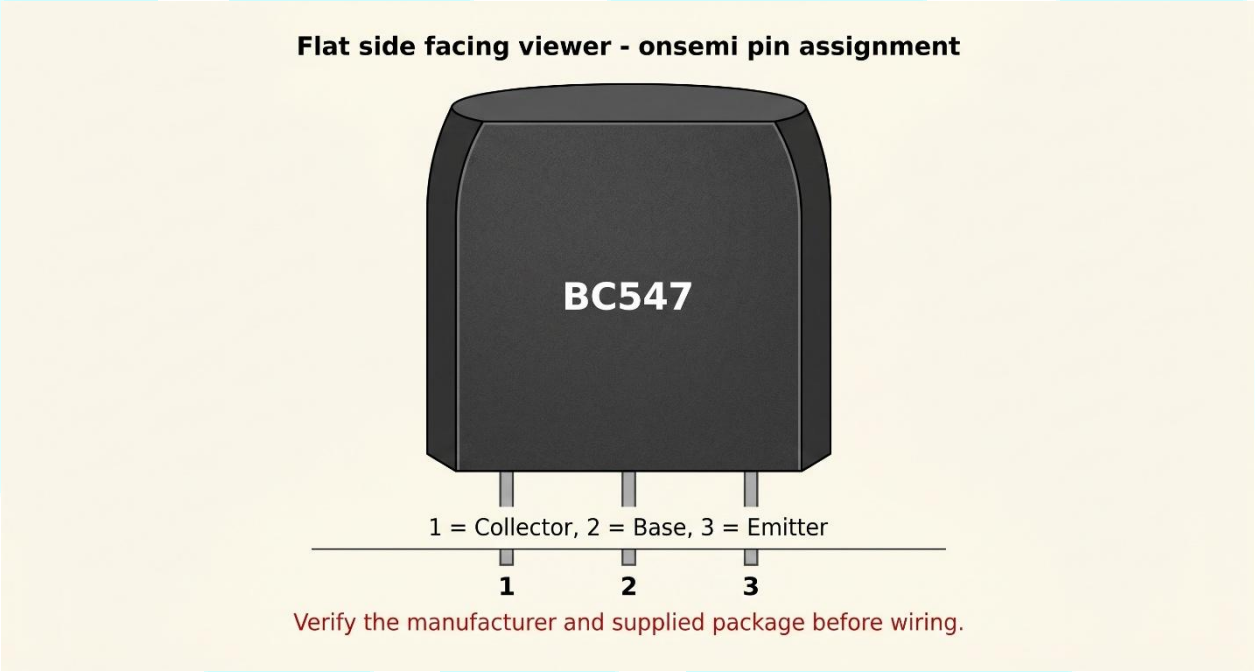


Figure 1. onsemi BC547 TO-92 pin assignment. Confirm the manufacturer of the supplied part.

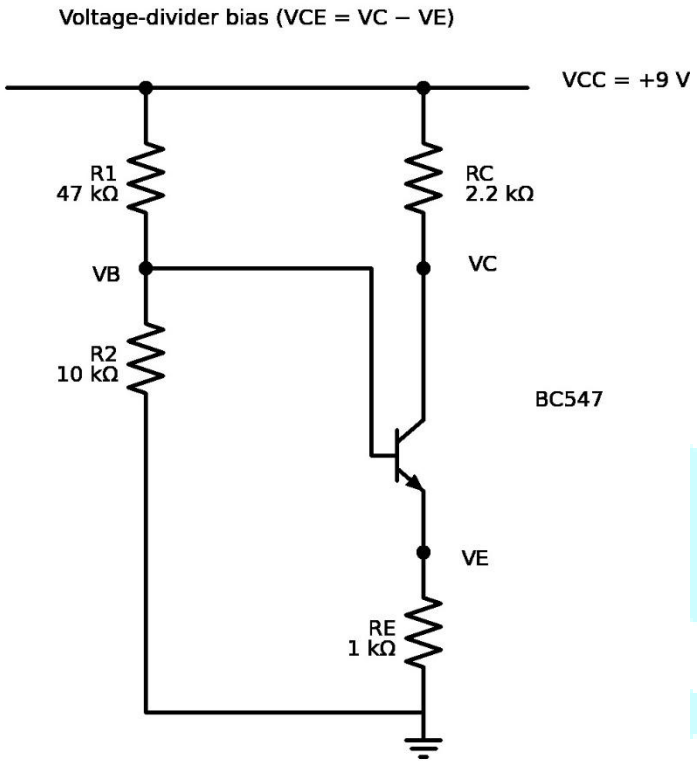


Figure 2. Voltage-divider bias circuit used in this experiment, with the RC branch connected directly to the collector terminal and the measurement nodes VB, VC, and VE marked.

3. Materials Used

Item	Minimum quantity / setting	Purpose
BC547 NPN transistors	2 if available	Variation test
R1 / R2	47 kΩ / 10 kΩ	Base divider
RC / RE	2.2 kΩ / 1 kΩ	Collector and emitter bias
DC supply	7, 9, and 11 V; current limited	Supply sweep
DMMs	2 preferred	Node voltages and currents
Breadboard and jumpers	1 set	Construction
Proteus or similar simulator	Pre-lab	Q-point comparison
Additional resistor	10 kΩ	Fault case RC = 10 kΩ

4. Procedure

Part A - Pre-calculation

1. Measure all resistor values. Using VCC = 9 V, calculate VTH and RTH.
2. Calculate the Q point for β = 100 and VBE = 0.70 V including base loading. Also calculate the unloaded-divider approximation and compare.
3. Calculate the two DC load-line intercepts.

Parameter	Loaded-divider calculation	Unloaded-divider approximation	Measured
VTH (V)		-	N/A (calculated parameter)
RTH (kΩ)		-	N/A (calculated parameter)
VB (V)			
VE (V)			
VC (V)			
VCE (V)			
IC (mA)			

Part B - Build and measure Q point

1. Build the voltage-divider bias circuit shown in Figure 2 with the supply off, and verify the exact transistor pinout using Figure 1 and the manufacturer datasheet.
2. Set 9 V and a 10 mA current limit. Measure VB, VE, VC, VCE, and the voltage drops across RC and RE.
3. Calculate IC from VRC/RC and IE from VRE/RE. Estimate IB = IE - IC and β = IC/IB only if the difference is above meter uncertainty.
4. Plot the measured Q point on the load line.

Part C - Supply sensitivity

1. Repeat node-voltage measurements at VCC = 7 V and 11 V without changing resistors.
2. Calculate the supply sensitivity across the tested range as $\Delta IC/\Delta VCC = [IC(11\ V) - IC(7\ V)] / 4\ V$ and $\Delta VCE/\Delta VCC = [VCE(11\ V) - VCE(7\ V)] / 4\ V$.
3. Check at each voltage that the transistor remains in the active region.

VCC (V)	VB	VE	VC	VCE	IC from RC	IE from RE	Region
7							
9							
11							

Part D - Device variation and fault cases

1. If a second BC547 is available, power off, replace the transistor with it, and repeat the 9 V measurements. If no second device is available, record this case as N/A.
2. Compare the change in IC and VCE with the transistor replacement. Explain why emitter feedback reduces β sensitivity.
3. Introduce one instructor-approved bias fault at a time: R1 open, R2 open, RE shorted, or RC increased to 10 kΩ. Note that R1 open removes the base drive and is the fault that pushes the stage toward cutoff. Predict the operating region, measure node voltages, and restore the circuit.

Case	VB	VE	VC	VCE	IC	Predicted / measured region
BC547 sample 1						
BC547 sample 2						
R1 open						
R2 open						
RE shorted						
RC = 10 kΩ						

5. Evaluation of Results

Discussion questions

1. How much did IC change when the transistor was replaced? Is the result consistent with a stable bias network?
2. Response:

   _____

   _____

3. Why does the unloaded-divider approximation overestimate or underestimate VB?
4. Response:

   _____

   _____

5. Which fault drives the transistor toward cutoff and which toward saturation? Use node voltages.
6. Response:

   _____

   _____

7. Is the 9 V Q point centered on the load line? Discuss available positive and negative output swing.
8. Response:

   _____

   _____

6. Safety Precautions

- Verify transistor pinout and supply polarity before power.
- Keep the current limit near 10 mA during initial tests.
- Power off before transistor replacement or fault insertion.
- Do not heat the transistor deliberately; temperature tests require a controlled procedure.

7. References

12. Auburn University ELEC 2210, BJT Transistors Laboratory.
13. onsemi, BC547 Family Datasheet.
14. R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed., 2012.
15. T.C. Ministry of National Education, Elektronik Elemanlar ve Devre Teorisi, course textbook.

EXPERIMENT 11: RC-Coupled Common-Emitter Amplifier and Frequency Response

1. Objective of the Experiment

To verify the DC operating point, measure midband gain and phase inversion, and obtain the frequency response of an RC-coupled BC547 common-emitter amplifier.

Learning outcomes

- Separate DC bias analysis from AC small-signal behavior.
- Prevent output clipping by selecting a suitable input amplitude.
- Measure voltage gain over logarithmically spaced frequencies.
- Determine lower and upper -3 dB frequencies when observable.

2. Theoretical Background

The common-emitter stage converts a small base voltage variation into a larger collector voltage variation with approximately 180° phase inversion. Coupling capacitors block DC while passing the signal. An emitter bypass capacitor, if used, increases AC gain while preserving DC feedback.

The gain is frequency dependent. Coupling and bypass capacitors dominate the low-frequency reduction; transistor junction capacitances and measurement loading dominate the high-frequency reduction. The -3 dB points occur where gain magnitude falls to 0.707 of the midband value.

Figure 1. onsemi BC547 TO-92 pin assignment. Confirm the manufacturer of the supplied part.

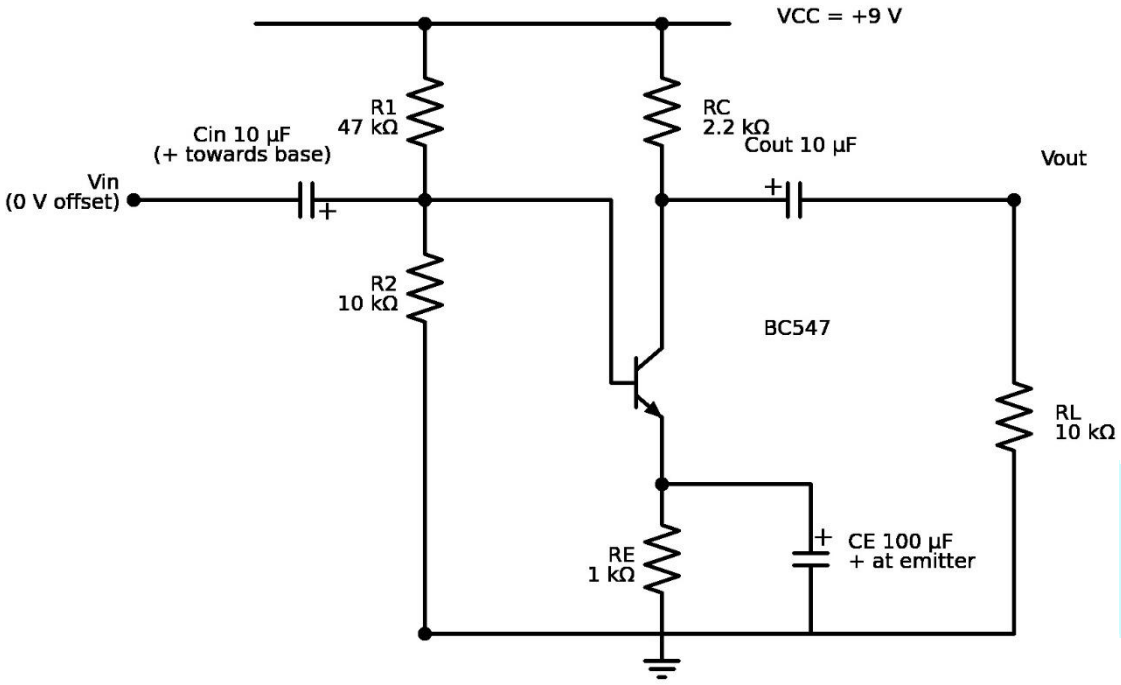


Figure 2. Complete RC-coupled CE stage with voltage-divider bias and a 10 kΩ load. CE is fitted and removed for the Part D bypass comparison.

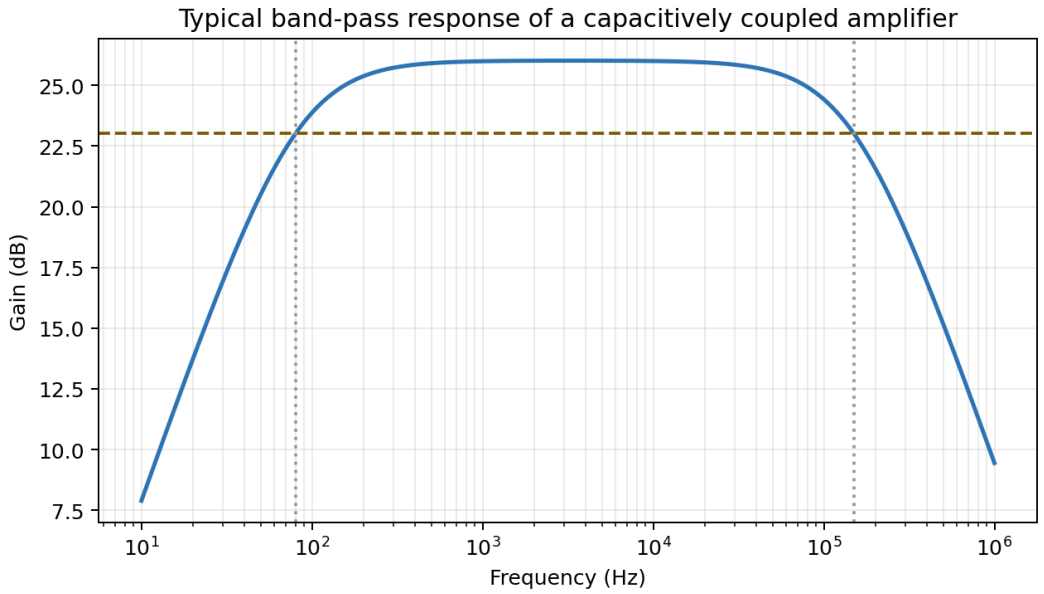


Figure 3. Typical response and -3 dB criterion. Actual corner frequencies depend on the built circuit and instruments.

3. Materials Used

Item	Minimum quantity / setting	Purpose
BC547 stage from Experiment 10	R1=47 kΩ, R2=10 kΩ, RC=2.2 kΩ, RE=1 kΩ	Bias
Coupling capacitors	Cin=Cout=10 µF, ≥25 V	DC isolation
Emitter bypass capacitor	100 µF, ≥25 V, required for the Part B and Part D comparisons	Gain change
Function generator	20 mVpp initial, sine	Small-signal input
Two-channel oscilloscope	1	Amplitude and phase
DC supply	9 V, current limited	Bias
Load resistor	10 kΩ	Defined load
Digital multimeter	1	DC operating-point measurements
Solderless breadboard and jumper wires	1 set	Amplifier assembly

4. Procedure

Part A - DC operating point and safe signal level

1. Build the complete amplifier with supply off. Verify electrolytic polarities from the expected DC voltages.
2. Apply 9 V. With the generator disconnected or set to zero AC, measure VB, VE, VC, and VCE. Confirm active-region bias.
3. Connect a 1 kHz sine input through Cin at 20 mVpp with the generator DC offset set to 0 V. Display Vin and Vout. Increase or decrease Vin so the output is clean and measurable without clipping.
4. Record the actual input amplitude and keep it constant during the sweep.

DC quantity	Expected from Exp. 10	Measured	Acceptable for active operation?
VB (V)			
VE (V)			
VC (V)			
VCE (V)			

Part B - Midband gain and phase

1. At 1 kHz, measure Vin,pp and Vout,pp with oscilloscope cursors. Calculate Av = Vout/Vin and gain in dB = 20 log10|Av|.
2. Measure time displacement Δt and calculate phase φ = 360° f Δt with the sign inferred from waveform order.
3. Record whether the output is inverted. Save a waveform with both zero references visible.
4. First complete the 1 kHz measurements without the emitter bypass capacitor C_E. Record the results in the "R_E unbypassed" row of the table.
5. Power off the circuit. Connect $C_E = 100\ \mu F$ in parallel with R_E, with its positive terminal connected to the emitter and its negative terminal connected to ground. Power on, confirm that the DC operating point has not changed significantly, and repeat the 1 kHz gain and phase measurements. Record the results in the "R_E bypassed with $100\ \mu F$" row.

Condition	Vin,pp	Vout,pp	|Av|	Gain (dB)	Δt	Phase
RE unbypassed						
RE bypassed with 100 µF						

Part C - Frequency sweep

1. Choose bypassed or unbypassed operation as directed. At each frequency, verify the input amplitude at the amplifier input rather than trusting the generator display.
2. Measure Vin,pp and Vout,pp at the listed logarithmic frequencies. Reduce generator amplitude only if clipping occurs and record any change.
3. Extend below 20 Hz or above 1 MHz if necessary and if equipment permits. Do not claim fH if the gain has not fallen by 3 dB.

f (Hz)	Vin,pp	Vout,pp	|Av|	Gain (dB)	Waveform / clipping note
20					
50					
100					
200					
500					
1k					
2k					
5k					
10k					

f (Hz)	Vin,pp	Vout,pp	|Av|	Gain (dB)	Waveform / clipping note
20k					
50k					
100k					
200k					
300k					
500k					
1M					

Part D - Corner frequencies and capacitor comparison

1. Determine the mean midband gain from several flat-region points. Calculate the -3 dB target.
2. Interpolate or take additional measurements near fL and fH. State if a corner lies outside the available range.
3. Power off the circuit and change to the opposite emitter-bypass condition used in Part C. Repeat the measurements at 50 Hz, 1 kHz, and 10 kHz. Compare the voltage gain values and explain the observed changes.

Bypass comparison (Part D, step 3): record the gain magnitudes for both emitter-bypass conditions at the three comparison frequencies.

f (Hz)	|Av| with RE unbypassed	|Av| with RE bypassed
50		
1 k		
10 k		

Corner frequencies and bandwidth:

Quantity	Result	Method / evidence
Midband gain (dB)		
-3 dB target (dB)		
fL (Hz)		
fH (Hz)		
Bandwidth (Hz)		

5. Evaluation of Results

Discussion questions

1. Why must the input amplitude be measured at every frequency?

   Response:

   _____

   _____

2. Does the output show 180° inversion at midband? Quantify from Δt.

   Response:

   _____

   _____

3. Which physical elements set fL and fH in this circuit?

   Response:

   _____

   _____

4. If fH is not reached, what is the scientifically correct way to report the result?

   Response:

   _____

   _____

6. Safety Precautions

- Verify DC bias before applying an AC signal.
- Observe electrolytic capacitor polarity; coupling-capacitor polarity follows the DC voltage on each side.
- Use a common approved ground for generator and oscilloscope.
- Keep the input small enough to avoid saturation and cutoff clipping.

7. References

1. Concordia University ELEC 312, RC-Coupled CE Amplifier Laboratory.
2. Auburn University ELEC 2210, BJT Transistors Laboratory.
3. R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed., 2012.
4. T.C. Ministry of National Education, Elektronik Elemanlar ve Devre Teorisi, course textbook.

EXPERIMENT 12: LM358 Voltage Follower, Inverting, and Non-Inverting Amplifiers

1. Objective of the Experiment

To build three fundamental LM358 closed-loop configurations on a single supply, verify gain and phase, and observe output-swing and frequency limitations.

Learning outcomes

- Identify LM358 power and signal pins from the datasheet.
- Create and decouple a mid-supply reference for AC signal processing.
- Measure follower, inverting, and non-inverting closed-loop gains.
- Distinguish ideal gain equations from finite bandwidth, slew rate, and output-swing limits.

2. Theoretical Background

With negative feedback and linear operation, an ideal op-amp is approximated by negligible input current and V+ ≈ V-. These rules apply only when the output is not saturated and the required rate of change is within the device capability.

For a single 9 V supply, a bipolar input signal cannot be centered at 0 V. A reference VREF = VCC/2 provides a signal midpoint. Voltages and gains are then interpreted as deviations around VREF. VREF is a bias reference, not the power-supply ground.

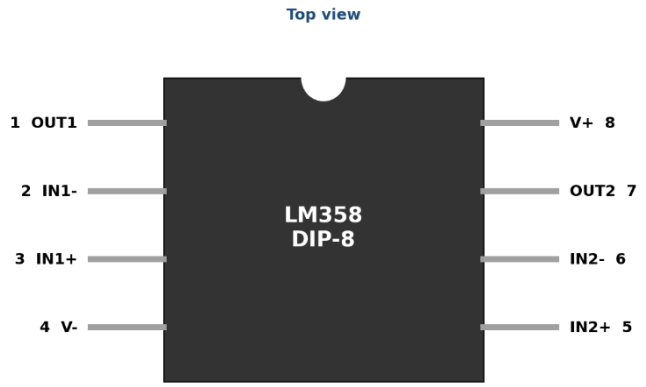


Figure 1. LM358 DIP-8 top-view pinout.

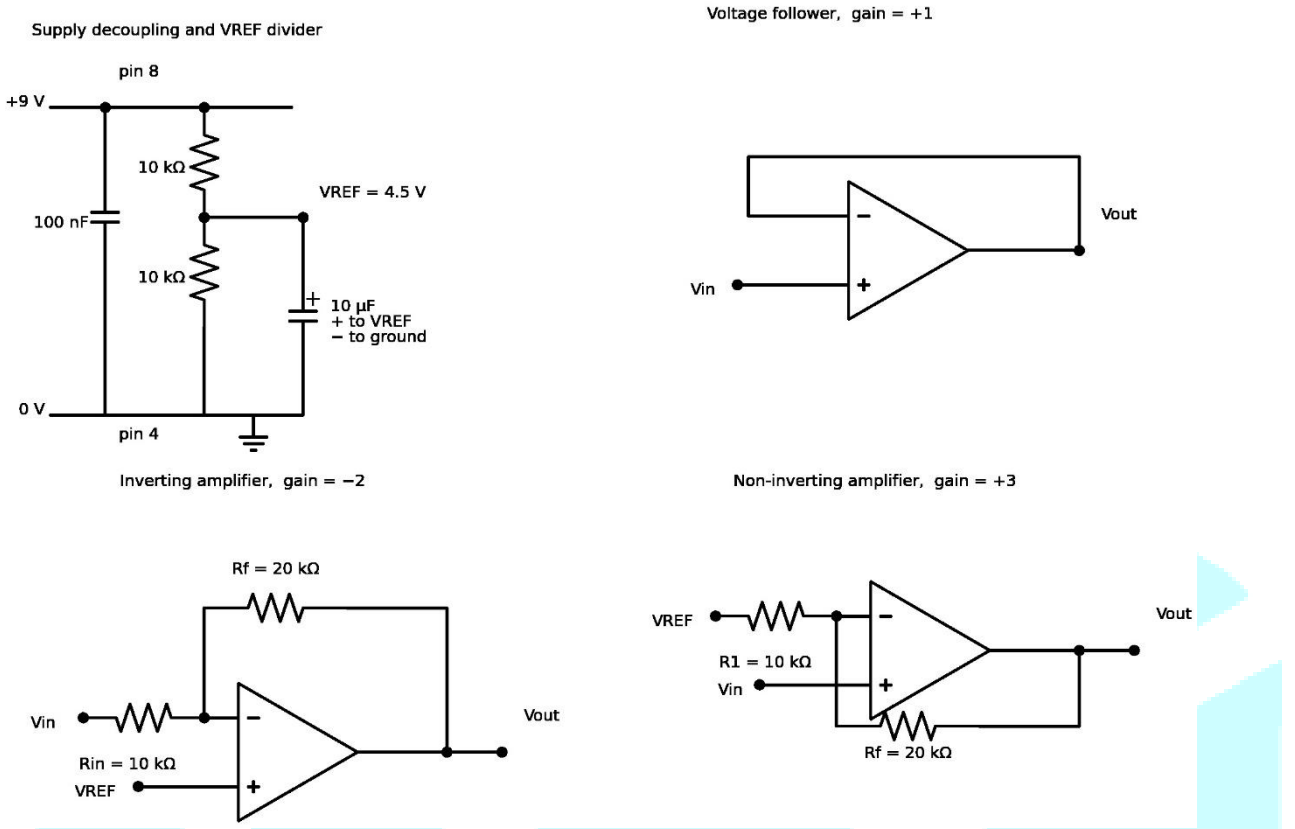


Figure 2. Supply decoupling and VREF divider, voltage follower, inverting amplifier (gain −2), and non-inverting amplifier (gain +3). Pin 8 is +9 V, pin 4 is 0 V, and all signals are biased around VREF = 4.5 V for single-supply operation.

3. Materials Used

Item	Minimum quantity / setting	Purpose
LM358 DIP-8	1	Dual op-amp
DC supply	9 V, current limited	Single supply
VREF divider	2 x 10 kΩ + 10 µF bypass	Mid-supply reference
Gain resistors	Rin=10 kΩ, Rf=20 kΩ; R1=10 kΩ, Rf=20 kΩ	Gains -2 and +3
Function generator	Sine, 0.5 Vpp around 4.5 V	Input
Two-channel oscilloscope and DMM	1 each	AC/DC measurements
100 nF decoupling capacitor	1	Supply bypass at IC
Solderless breadboard and jumper wires	1 set	Op-amp assembly

4. Procedure

Part A - Pinout, supply, and VREF

1. From the datasheet, draw the DIP-8 top view and label OUT1, IN1-, IN1+, V-, V+, OUT2, IN2-, and IN2+.
2. With power off, place the IC across the breadboard center gap. Connect pin 8 to +9 V, pin 4 to ground, and 100 nF directly between pins 8 and 4.

3. Build a 10 kΩ / 10 kΩ divider from 9 V to ground and bypass its midpoint with 10 µF (+ to VREF, − to ground). Wait for settling, then measure VREF unloaded.
4. Connect a 10 kΩ test load from VREF to ground, wait for settling, and measure VREF again; the ideal loaded-divider value is 3.00 V. Then remove it. Explain why a simple divider is not an ideal low-impedance reference.
5. Do not leave the unused LM358 amplifier inputs floating. If amplifier 1 is used for the experiment, connect pin 5 to VREF and connect pin 7 to pin 6 so that amplifier 2 operates as a voltage follower at VREF.

VREF condition	Calculated	Measured	Difference / interpretation
Unloaded	4.50 V		
With 10 kΩ load			
After load removed	4.50 V		

Part B - Voltage follower

1. Apply DC input levels of 1, 2, 4.5, 6, and 7 V using the function-generator offset or another instructor-approved source. Verify each input with the DMM. Test 8 V only as an instructor-approved limit case and label it as outside the expected linear common-mode range.
2. Record output and error Vout - Vin. Identify where the output ceases to follow accurately.
3. Apply a 1 kHz, 0.5 Vpp sine centered at 4.5 V. Verify gain and phase.

Vin DC (V)	Vout (V)	Error (mV)	Linear / limited
1			
2			
4.5			
6			
7			
8			

Part C - Inverting amplifier about VREF

1. Build Rin = 10 kΩ and Rf = 20 kΩ. Connect the non-inverting input to VREF. Apply a sine whose DC level is VREF.
2. At 100 Hz, 1 kHz, and 10 kHz, measure input and output amplitudes and phase. Expected small-signal gain about VREF is -2.
3. Increase input amplitude gradually until clipping first appears. Record upper and lower output limits.

f	Vin,pp	Vout,pp	Measured gain	Phase	Clipping?
100 Hz					
1 kHz					
10 kHz					

Part D - Non-inverting amplifier and bandwidth

1. Build the non-inverting amplifier with R1 = 10 kΩ from the inverting node to VREF and Rf = 20 kΩ from output to the inverting node. Expected gain is +3.

2. Begin the frequency-response measurement with approximately 0.1 Vpp input centered at VREF. Verify the actual input amplitude at every frequency and reduce it if necessary so that the output remains sinusoidal and free from slew-rate distortion.
3. Measure phase qualitatively and note waveform distortion. If the -3 dB point is not reached, report a lower bound rather than inventing a bandwidth.
4. For the slew-rate test, first record Vout,pp,max, the largest undistorted output amplitude obtained at low frequency. Take the slew rate SR from the datasheet of the device actually used (0.3 V/µs typical for a standard LM358) and choose one stated test frequency above f = SR / (π Vout,pp,max), so that the slew-rate limit is reached before the output-swing limit; verify that this frequency is still inside the closed-loop bandwidth, otherwise the amplitude falls off before slewing can be seen. Then increase the output amplitude at that frequency until slew-related distortion first appears. Distinguish the two mechanisms: amplitude clipping flattens the peaks at fixed levels that do not move with frequency, whereas slew-rate limiting turns the sine into a triangular shape whose sloped edges get worse as frequency increases. Record f and Vout,pp, and compare the requirement SRrequired = π f Vout,pp with the LM358 datasheet.
5. Use SR in V/s and Vout,pp,max in volts to calculate frequency in Hz. For example, 0.3 V/µs = 300,000 V/s.

f	Vin,pp	Vout,pp	Gain	Gain (dB)	Phase / distortion
100 Hz					
1 kHz					
10 kHz					
30 kHz					
100 kHz					
200 kHz					
300 kHz					
500 kHz					
1 MHz					

Part E - Summary comparison

Configuration	Ideal gain	Measured midband gain	Phase	Observed limit
Follower	+1		0°	
Inverting	-2		≈180°	
Non-inverting	+3		≈0°	

5. Evaluation of Results

Discussion questions

1. Why is VREF required for these single-supply AC tests?

   Response:

   _____

   _____

2. For each amplifier, compare measured and ideal gain and identify the dominant source of discrepancy.

   Response:

   _____

   _____

3. Why does the output clip asymmetrically near the supply rails?
   Response:
   _____
   _____

4. Separate gain-bandwidth limitation from slew-rate limitation using your measurements.
   Response:
   _____
   _____

6. Safety Precautions

- Confirm LM358 orientation and pins 4/8 before applying power.
- Place the 100 nF decoupling capacitor close to the IC supply pins.
- Do not short the output to ground, VREF, or a supply rail.
- Keep input voltage within the powered circuit's allowed range and power off before rewiring.

7. References

1. MIT OpenCourseWare 6.002, Operational Amplifier Circuits.
2. Texas Instruments, LM358 Dual Operational Amplifier Datasheet and Product Page.
3. R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed., 2012.
4. T.C. Ministry of National Education, Elektronik Elemanlar ve Devre Teorisi, course textbook.